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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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Sheet

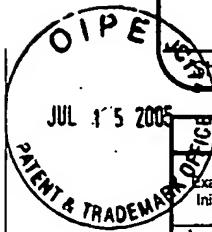
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of

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Application Number	10/003,184
Filing Date	10/30/2001
First Named Inventor	Frederic Reblewski
Art Unit	2123
Examiner Name	Kandasamy Thangavelu
Attorney Docket Number	003921.00070

JUL 15 2005



U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number - Kind Code ³ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
KJN		US- 5,265,894	07-2001	Reblewski et al.	
KJN		US- 5,596,742	01-1997	Agarwal et al.	
KJN		US- 5,663,900	09-1997	Bhandari et al.	
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KJN		US- 5,821,773	10-13-1998	Norman et al.	
KJN		US- 5,940,603	08-1999	Huang, Thomas B.	
KJN		US- 5,999,725	12-1999	Barbier et al.	
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KJN		US- 6,377,912	04-2002	Sample et al.	
KJN		US- 2002/0055828	05-2002	Swoboda et al.	
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KJN		US- 6,625,793	09-2003	Sample et al.	
KJN		US- 2002003/0182641	09-2003	Yang, Sei-Yang	
KJN		US- 2003/0179712	09-2003	Kobayashi et al.	
KJN		US- 2004-0034841-A1	02-19-2004	Reblewski	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
KJN		EP 0,651,343 A1	05-03-1995	Quickturn Systems Inc.		

Examiner Signature

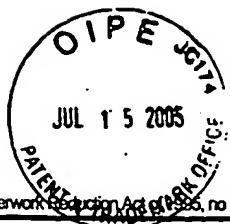
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PTO/SB/08b (08-03)

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Art Unit	2123
Examiner Name	Kandasamy Thangavelu

Attorney Docket Number

003921.00070

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
KJN		Erhard et al., W. First Steps-Towards a Reconfigurable Asynchronous System, IEEE International Workshop on Rapid System Prototyping, 1999, pgs. 28-31	
KJN		Kocan et al., F. Concurrent D-Algorithm on Reconfigurable Hardware, IEEE/ACM International Conference on Computer-Aided Design, 1999, Digest of Technical Papers, pgs. 152-155	
KJN		Clos, Charles, "A study of Non-Blocking Switching Networks," The Bell System Technical Journal, March 1953, pgs. 406-424	
KJN		Bosi et al., B. Reconfigurable Pipelined 2-D Convolvers for Fast Digital Signal Processing, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 7, Issue 3, Sept. 1999, pgs. 299-308	
KJN		Ejnioui et al., A. Design Partitioning on Single-Chip Emulation Systems, 13 th International Conference on VLSI Design, 2000, pgs. 234-239	
KJN		Jean, J.S.N., et al., "Dynamic Reconfiguration to Support Concurrent Applications," IEEE Transactions on Computers, June 1999, IEEE, USA, vol. 48, No. 6, pgs. 591-602	
KJN		Snider, G., "The Teramac Compiler," Nov. 29, 1993, pgs. 1-51	
KJN		Babb, J. et al., "Logic Emulation with Virtual Wires," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 1997, pgs. 1-20	

Examiner Signature

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8/16/05

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